ANURAG YADAV

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Objective

To reach the zenith of organization hierarchy through continuous self-development, learning and experiencing the critical aspects of technology & management.

Education Qualification

NAME OF DEGREE	YEAR	NAME OF THE INSTITUTE/UNIVERSITY	MARKS/GRADE
Ph.D. Pursuing, Electronic Engineering (VLSI)	Since 22/08/2019	Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow (Under Homi Bhabha Research cum Teaching Fellowship Scheme) Institute of Engineering and Technology, Lucknow	Pursuing
M.E. (**ECE**) Regular Full Time	2014-2016	National Institute of Technical Teachers Training and Research, Chandigarh /Panjab University, India	8.35 CGPA
B. Tech (**ECE**)	2004-2008	Northern India Engineering College /Uttar Pradesh Technical University Lucknow, India	66.46%
Class XII	2002	R.L.B. School, Indira Nagar, Lucknow (CBSE Board), Uttar Pradesh, India	66.80%
Class Xth	2000	R.L.B. School, Indira Nagar, Lucknow (CBSE Board), Uttar Pradesh. (India)	69.00%

Projects

- Optimized Design of Column Level ADC for CMOS Imager using Switched Capacitor Technique at *National Institute of Technical Teachers Training and Research (NITTTR) Chandigarh and Semi-Conductor Laboratory (SCL), Mohali*.
- Multi Channel Remote Control System at *Northern India Engineering College, Lucknow*.

Summer Internship

- Summer Training In SU-30 at HAL(2007)
- Summer Training In VHDL Design Educational And Training completed project on "Digital Clock" at VEDANT VLSI Design Educational And Training (2006)

Work Experience

ORGANISATION	DEPARTMENT	POSITION HELD	DURATION	FROM	TO
Institute of Engineering and Technology, Lucknow	M.Tech, Microelectronics Programme, ECD	Assistant Professor	2 Year and 5 months	05/12/2022	Till date
Institute of Engineering and Technology, Dr. A.P.J. Abdul Kalam Technical University, U.P., Lucknow	Electronics & Communication Engineering	Teacher Fellow	3 Year	22/08/2019	22/08/2022
University Institute of Engineering & Technology, Babasaheb Bhimrao Ambedkar University, Lucknow (Central University)	Electronics & Communication Engineering	Resource Person	04 months	24/08/2018	17/12/2018
Institute of Engineering and Technology, Dr. Ram Manohar Lohia Avadh University, Faizabad (State University)	Electronics & Communication	Guest Faculty	09 months	04/09/2017	14/06/2018
Sherwood College of Engineering Research & Technology (SCERT), Barabanki	Electronics & Communication Engineering	Lecturer	3 Year 10 months	03/08/2010	30/06/2014

Core Competencies

Academic Accolades

- ⇨ Command over PCB and Workshop, Basic Electronics Lab, CAD for Electronics Lab**,** VLSI Design Lab.
- ⇨ Member, Exam Cell Committee at SCERT Barabanki.
- ⇨ Class co-ordinator at SCERT Barabanki.

Accolades

- ⇨ Qualified GATE 2019 and UGC NET December 2023.
- ⇨ I have achieved Top 1 %(99 Percentile) in 4th National IT Aptitude Test 2008.
- ⇨ I got Academic honour certificate in Intermediate.

Areas of Interest

VLSI technology /Design, Digital Electronics, Electromagnetic field theory

Computing Skills

- ⇨ **Programming**: C, MATLAB, Assembly language programming, VHDL
- ⇨ **Operating System**: Windows
- ⇨ **Platform**: EAGLE (PCB designing tool), DSCH, Microwind (VLSI Circuit design), Virtuoso and Encounter tool in Cadence environment in VLSI design
- ⇨ **Typographic**: Microsoft Office
- ⇨ **Typing**: Hindi (Mangal Font), English

Publications

Published/Accepted Papers

International Journals:

1. Anurag Yadav and Subodh Wairya "Design and Analysis of Low Power and High Speed Dynamic Comparator with Transconductance Enhanced in Latching stage for ADC Application", Journal of Circuits, Systems, and Computers (JCSC), 2024, vol 33, no. 11, pp. 1-22, DOI: https://doi.org/10.1142/S0218126624501986, **SCIE.**

2. Anurag Yadav and Subodh Wairya, "Charge Shared based Low Power and High-Speed Dynamic Comparator for High Frequency Analog Signal Processing Architecture", Integration, Vol. 103, 102426, 2025, **SCIE**, https://doi.org/10.1016/j.vlsi.2025.102426.

3. Anurag Yadav and Subodh Wairya, "Design and Analysis of Low Power, High Speed and Sensing Small Differential Input Signal of Dynamic Comparator with Transconductance Improved Latching Stage", Journal of Circuits, Systems, and Computers (JCSC), **SCIE (ACCEPTED)**.

4. Saqib, Mohd, Subodh Wairya, and **Anurag Yadav**. "A 6.7 GHz, 89.33 μW power and 81.26% tuning range dual input ring VCO with PMOS varactor." Journal of Circuits, Systems and Computers (2023), vol. 32, no. 12, pp. 1-15, DOI: https://doi.org/10.1142/S0218126623501992, **SCIE.**

5. Anurag Yadav and Subodh Wairya, "Performance and Area Optimization of SRAM Cell in Nanocomputing Application", International Journal Of Computing and Digital System, University of Bahrain, vol. 11, no.1, Mar-2022 pp. 1009-1026, https://dx.doi.org/10.12785/ijcds/110182, **(SCOPUS Indexed).**

6. Mishra, Vivek, **Anurag Yadav**, and Subodh Wairya. "Design of Compensated Supply Circuit Topology for a Ring Oscillator." Int. J. Com. Dig. Sys 12.1, pp.1005-1017, (2022). DOI: https://dx.doi.org/10.12785/ijcds/120181, University of Bahrain, **(SCOPUS Indexed).**

7. Anurag Yadav, Rajesh Mehra, Deep Sehgal and H.S. Jatana, "High Performance Column Level ADC for CMOS Imager using Switched Capacitor Technique", International Journal of Advanced Research in Computer and Communication Engineering, Vol. 5, Issue 7, pp. 451-456, July 2016.

8. Anurag Yadav, Rajesh Mehra and Deep Sehgal "Optimized Design of Column Level ADC for CMOS Imager using 180 nm Technology", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), Vol. 6, Issue 4, pp. 20-25, July-August 2016.

9. Anurag Yadav, Rajesh Mehra, "Efficient Layout Design of 4-Bit Full Adder Using Transmission Gate", International Journal of Computer Trends & Technology (IJCTT), Volume 23, No. 3, pp. 116-119, May 2015.

Book Chapters:

1. Nashra Khalid, **Anurag Yadav** and Subodh Wairya, "Performance analysis of various fast and low power dynamic comparators", International Conference on Intelligent Systems and Smart Infrastructure (ICISSI)", jointly Organised By Shambhunath Institute of Engineering and Technology, Prayagraj (U.P.) India& Institute of Engineering and Technology, Lucknow (U.P.) India & Manipal University Jaipur, India on 21st & 22nd May 2022, **(Best Paper Award),** / Intelligent Systems and Smart Infrastructure, Taylor & Francis Group, London, ISBN 978-1-032-41287-0, pp. 64-71, DOI: 10.1201/9781003357346-9**.**

2. Kunal Kumar, **Anurag Yadav** and Subodh Wairya, "Design and Analysis of High speed and Low Power Dynamic Comparator", International Conference on Intelligent Systems and Smart Infrastructure (ICISSI)", 2022, jointly Organised By Shambhunath Institute of Engineering and Technology, Prayagraj (U.P.) India& Institute of Engineering and Technology, Lucknow (U.P.) India & Manipal University Jaipur, India on 21st & 22nd May 2022 / Intelligent Systems and Smart Infrastructure, Taylor & Francis Group, London, ISBN 978-1-032-41287-0, pp. 107-117, DOI: 10.1201/9781003357346-9**.**

International Conferences:

1. Agyenya Anand, Anurag Yadav, Subodh Wairva, "Performance Analysis of Fast & Power Efficient Dynamic Comparator Topologies", 2024 2nd International Conference on Device Intelligence, Computing and Communication Technologies (DICCT), pp. 654-658, **DOI:** 10.1109/DICCT61038.2024.10533168, **(Published in IEEE Xplore Digital Library).**

2.Saxena, Abhinav, **Anurag Yadav**, and Subodh Wairya. "Design Analysis of 3-Bit Flash ADC using Low-Offset and Low-Power Opamp." 2023 10th International Conference on Signal Processing and Integrated Networks (SPIN). IEEE, pp.502-507, 2023, **DOI:** 10.1109/SPIN57001.2023.10116426 **(SCOPUS Indexed and Published in IEEE Xplore Digital Library).**

3. Abhinav Saxena, **Anurag Yadav**, "Subodh Wairya, "Design Analysis of an Energy-Efficient Low-Power Dynamic Comparator Using NMOS based Preamplifier", 14th International Conference On Computing, Communication And Networking Technologies (ICCCNT) July 6th-8th, 2023, IEEE, **(SCOPUS Indexed and Published in IEEE Xplore Digital Library)**.

4.Saqib, Mohd, Subodh Wairya, and **Anurag Yadav**. "Performance Analysis of Differential Dual Stage Delay Cells of VCO." International Conference on VLSI, Communication and Signal processing. Singapore: Springer Nature Singapore, 2022.

5. Kunal, **Anurag Yadav**, and Subodh Wairya. "Design of Ultralow-Power and High-Speed Comparator Using Charge Sharing Technique." International Conference on VLSI, Communication and Signal processing. Singapore: Springer Nature Singapore, 2022.

6. A. Yadav, N. Rai, A. Verma and S. Wairya, "Design of Flash ADC using low offset comparator for analog signal processing application," 2021 8th International Conference on Signal Processing and Integrated Networks (SPIN), 2021, pp. 76-81, doi: 10.1109/SPIN52536.2021.9566050, organized by Amity University, Noida, on 26-27 August 2021, **(SCOPUS Indexed and Published in IEEE Xplore Digital Library).**

7. Nivedita Rai, **Anurag Yadav** and Subodh Wairya, "Design of a High Speed and Low Power Charge Shared Based Dynamic Comparator for ADC Application", IEEE,1st International Conference on Advances in Computing and Future Communication Technologies (ICACFCT), 2021, pp. 125-130 **DOI:** 10.1109/ICACFCT53978.2021.9837362, organized by Meerut Institute of Engineering and Technology, Meerut, India on 16-17 December, 2021, (**Published in IEEE Xplore Digital Library).**

8. Anurag Yadav, "Area Efficient 4-Bit Full Adder Design using CMOS 90 nm Technology**",** Int. Journal of Electrical & Electronics Engg., Vol. 2, No. 1, pp. 45-48, 2015 / 1st International conference on Electronic Design Innovations & Technologies (EDIT), 2015 organized by Department of Electronics & Communication Engineering NITTTR at NITTTR, Chandigarh.

9. Anurag Yadav, Rajesh Mehra " FPGA based IIR Filter Design Analysis for Different Orders" Journal of Basic and Applied Engineering Research , Vol. 1, No. 12, pp. 106-109, 2014 / 6th international conference on Innovative trends in mechanical, Manufacturing, Automobile, Aeronautical Engineering and Applied Physics (ITMAEAP), 2014, organized by Social Welfare Foundation in association with Krishi Sanskriti at Jawaharlal Nehru University.

NPTEL Courses/FDP/STC Attended

NPTEL Courses

S.NO.	DURATION	TOPIC	ORGANIZER
1.	January to April 2020 (12 week course)	Analog IC Design	IIT Madras
2.	September to December 2020 (12 week course)	Digital VLSI Testing	IIT Kharagpur
3.	January to April 2021 (12 week course)	Basic Electronics	IIT Bombay
4.	Jan-Apr 2025 (12 week course)	Integrated Circuits, Mosfets, OP-Amps and their Applications	IISc Banglore
5.	Jan-Mar 2025 (08 week course)	CMOS Digital VLSI Design	IIT Roorkee
6.	Jan-Feb 2025 (04 week course)	Python for Data Science	IIT Madras

Short Term Course (STC)

S.NO.	DURATION	TOPIC	ORGANIZER
1.	06.02.2021 to 10.02.2021 (One Week)	Sustainable Trends in Energy & Environment (STEE-2021)	Department of Chemical Engineering, Institute of Engineering & Technology, Lucknow, Uttar Pradesh, India

Faculty Development Programme (FDP)

S.NO.	DURATION	TOPIC	ORGANIZER
1.	19.10.2019 to 23.10.2019 (One Week)	Advances in Renewable and Bioenergy	Department of Chemical Engineering, IET Lucknow, held at Institute of Engineering & Technology. Lucknow Uttar Pradesh, India
2.	22.06.2020 to 26.06.2020 (One Week)	Electrical Vehicles: New Trends and Technologies	Department Electrical and Electronics Engineering. ABES Engineering College, Gaziabad, India
3.	13.07.2020-18.07.2020 (One Week)	Recent Trends in Electronics & Communication	Department of Electronics & Communication, Balaji Institute of Technology & Science, Telengana, India
4.	18.07.2020 to 25.07.2020 (8 Day)	Internet of Things	Department of Information Technology, Easwari Engineering College, Chennai, India
5.	31.08.2021 to 4.09.2021 (One Week)	Emerging Technologies of Opto-VLSI and its applications	Department of Electronics and Communication Engineering, Meerut Institute of Engineering & Technology in association with IEEE student Branch MIET Meerut and ENTUPLET Technologies, Meerut India
6.	17.07.2023 to 22.07.2023 (One Week)	Recent Trends in Organic Devices	Department of Electronics and Communication Engineering, School of Engineering, Presidency University, Bangalore, India
7.	0.3.02.2025 to 07.02.2025 (One Week)	Nanotechnology for VLSI: Fabrication and Challenges	Jointly organized by Electronics and ICT Academy, NIT Patna and Malla Reddy College of Engineering and Technology, Hyderabad, Telangana

Seminar and Conference Attended/Presented

- ⇨ Presented paper in "**All India Seminar on GREENS**", 2025, organized IET Lucknow and IEI UPSC, Lucknow on 4th and 5th February 2025.
- ⇨ Participated in the event, **"Empowering Engineering Education: The Role of IEEE Content"** jointly Organised by EBSCO & IEEE, on 16th June 2023 at Novotel Lucknow.
- ⇨ Participated in "**International Conference on Intelligent Systems and Smart Infrastructure (ICISSI)**", 2022, jointly Organised By Shambhunath Institute of Engineering and Technology, Prayagraj (U.P.) India& Institute of Engineering and Technology, Lucknow (U.P.) India & Manipal University Jaipur, India on 21st & 22nd May 2022.
- ⇨ Presented paper in "**8th International Conference on Signal Processing and Integrated Networks (SPIN)**", 2021, organized by Amity University, Noida, on 26-27 August 2021.
- ⇨ Presented paper in "**1st International Conference on Advances in Computing and Future Communication Technologies (ICACFCT)**", 2021, organized by Meerut Institute of Engineering and Technology, Meerut, India on 16-17 December, 2021.
- ⇨ Participated in "**International conference"** on "**Contemporary computing and applications (IC3A 2020)"**, held on 5-7 February 2020 at Dr. A.P.J. Abdul Kalam Technical Uttar Pradesh India.
- ⇨ Participated in "**International conference"** on "**Defence and Space Technologies, ICDST 2019"**, organized by department of Electronics and communication Engineering at Institute of Engineering and Technology, an autonomous constituent institute of Dr. A.P.J. Abdul Kalam Technical Uttar Pradesh India on 23-25 August, 2019.
- ⇨ Participated in "**International Seminar"** on "**Future Scope Robotics and Space Science"** organized by Electronics and Communication Engineering Department in Association with Enovate Skill (NITTTR Start – up) on 27.05.2016 (One Day) at NITTTR, Chandigarh (U.T.)
- ⇨ Presented paper in "**1st International conference on Electronic Design Innovations & Technologies (EDIT)**", 2015 organized by Department of Electronics & Communication Engineering NITTTR at NITTTR, Chandigarh.
- ⇨ Presented paper in "**6th international conference on Innovative trends in mechanical, Manufacturing, Automobile, Aeronautical Engineering and Applied Physics (ITMAEAP)"**, 2014, organized by Social Welfare Foundation in association with Krishi Sanskriti at Jawaharlal Nehru University.

- ⇨ Attended **All India Seminar on "communication Convergence"** organised by IE(I), U.P. State Centre, Lucknow, IETE, Lucknow Centre IE(I), Aparna Local Centre at IE(I) U.P. State Centre, Engineers Bhawan, River Bank Colony, Lucknow-226018 on September 8-9, 2007.

Work Shop Attended

- ⇨ Actively participated in the workshop on "**ROBUST AND RELIABLE VLSI CIRCUIT DESIGN**", Organised by IEEE CASS SBC, IIT Roorkee from 28th February to 02nd March 2025.
- ⇨ Participated in the event, "**Empowering Engineering Education: The Role of IEEE Content**" jointly Organised by EBSCO & IEEE, on 16th June 2023 at Novotel Lucknow.
- ⇨ Attended workshop on "**Applications of Machine Learning in Signal, Image & Computer Vision - AMALGAM 2021**" conducted and organised by IEEE Young Professionals Affinity Group UP Section, IEEE Signal Processing Society UP Chapter and BTKIT Dwarahat, Uttarakhand on 27 Dec to 31 Dec 2021.
- ⇨ Attended one week national workshop on "**AI & ML**" conducted by department of computer science and engineering collaboration with Chalapath institute of engineering & Technology (CSI) , Andhra Pradesh. from 13.07.2020 to 18.07.2020.
- ⇨ Attended workshop on "**Outcome Based Accreditation For Undergraduate Engineering Programs**" 9 March to 10 March, 2018 jointly organized by I.E.T., DR. Ram Manohar Lohia Avadh University Faizabad (U.P.) & DR. Ambedkar Institute of technology, Bangalore (Karnataka) at IET Campus Faizabad.
- ⇨ Attended two days workshop on "**2G and 3G**" conducted by Electronics & Communication Engineering Department of NITTTR Chandigarh from 3rd September to 4th September 2015.
- ⇨ Attended two days workshop on "**Signal Processing Tools & Techniques**" organized by Department of Electronics & Communication Engineering, Institute of Engineering & Technology, Dr. Ram Manohar Lohia Avadh University, Faizabad (U.P.) from 05 January to 06 January, 2018 at IET Campus Faizabad.

Webinar Attended

- ⇨ Attended webinar on "**Resistive switching technology for next-generation applications**"on 13th June 2020 organized by Centre For Advanced Studies, Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow.
- ⇨ Attended webinar on "**Leveraging Technology in Education**", on 0.1.05.2020 organized by Mc Graw Hill.

Extra Curricular Activities

- ⇨ Participates actively in "**All** India **Seminar on GREENS**", 2025, organized IET Lucknow and IEI UPSC, Lucknow on 4th and 5th February 2025.
- ⇨ Jury member for **E-Auction** on IEEE DAY on 5th October 2024, Organized by ECD, IET Lucknow under IEEE Student Branch.
- ⇨ Jury member for "**Advertisement Mania"** on IEEE DAY on 5th October 2024, Organized by ECD, IET Lucknow under IEEE Student Branch.
- ⇨ Participating in "**split free India Movement**" during June – August 2020 to prevent spreed of COVID-19 organized by Alamelu Charitable Foundation supported by TATA Trusts.
- ⇨ Participating in "Kargil Vijay Diwas Quiz" organized by Ministry of Human Development & My Gov.
- ⇨ Volunteered at "**5th National Organic Farming Convention**" on "**Mainstreaming Organic Farming**" organized from 28th February to 2nd March, 2015 at NITTTR Chandigarh.
- ⇨ Volunteered at "**4th National Abilympics**" organized from 3rd November to 5th November 2014 at NITTTR Chandigarh.
- ⇨ Participated in "**Young Business Leaders Program"** on "**Socially Responsible Business"** conducted by UNESCAP-EBAC Bangkok, CPSC Manila, NITTTR Chandigarh from 19 February to 20 February 2016 at NITTTR, Chandigarh.
- ⇨ Volunteered at **"Master's Training Program on Yoga"** Organized by AICTE in association with S- Vyasa on April 9, 2016 for International Day of Yoga (June 21, 2016) at NITTTR, Chandigarh.

Personal Dossier

Date of Birth : 18 May 1985
Address : 3/397 Vivek Khand-3, Gomti Nagar, Lucknow, Uttar Pradesh, Pin Code-226010
Linguistic Abilities: English & Hindi

Declaration:
I, hereby, declare that the particulars given in this document are true and complete to the best of my knowledge and belief.

Date: 08.05.2025 **(Anurag Yadav)**